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# TRANSMITTAL FORM

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| | |
|---|---|
| Application Number | 09/542,783 |
| Filing Date | April 4, 2000 |
| First Named Inventor | Whitman et al. |
| Group Art Unit | 2823 |
| Examiner Name | B. Kebede |
| Attorney Docket Number | 2269-4294US (98-1208.00/US) |

**ENCLOSURES** *(check all that apply)*

- ☒ Postcard receipt acknowledgment (attached to the front of this transmittal)
- ☒ Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- ☐ Preliminary Amendment
- ☐ Response to Restriction Requirement/Election of Species Requirement dated
- ☐ Amendment in response to office action dated
- ☐ Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- ☐ Additional claims fee - Check No. in the amount of $
- ☐ Letter to Chief Draftsman and copy of FIGS. with changes made in red
- ☐ Transmittal of Formal Drawings
- ☐ Formal Drawings ( sheets)
- ☐ Information Disclosure Statement, PTO/SB/08A (08-00); ☐ copy of cited references
- ☐ Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of $180.00
- ☐ Associate Power of Attorney
- ☐ Petition for Extension of Time and Check No. in the amount of $
- ☐ Petition
- ☒ Appeal Brief (18 pages) with Claims Appendix (4 pages); Check no. 8432 in the amount of $500.00
- ☐ Certified Copy of Priority Document(s)
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- ☐ Terminal Disclaimer
- ☐ Terminal Disclaimer
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Remarks

**The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.**

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

| | |
|---|---|
| Firm *or* Individual name | Brick G. Power — Registration No. 38,581 |
| Signature | Brick G. Power |
| Date | September 29, 2005 |

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PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

**In re Application of:**

Whitman et al.

**Serial No.:** 09/542,783

**Filed:** April 4, 2000

**For:** SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

**Confirmation No.:** 6870

**Examiner:** B. Kebede

**Group Art Unit:** 2823

**Attorney Docket No.:** 2269-4294US (98-1208.00/US)

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**APPEAL BRIEF**

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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## I. REAL PARTY IN INTEREST

U.S. Serial No. 09/542,783, the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc.. The assignment has been recorded with the United States Patent & Trademark Office (hereinafter the "Office") at Reel No. 10729, Frame No. 0057. Accordingly, Micron Technology, Inc. is the real party in interest to the referenced appeal.

## II. RELATED APPEALS AND INTERFERENCES

The final rejections in U.S. Application Serial No. 09/944,230, a divisional of the '783 Application, are currently on appeal before the Board of Patent Appeals and Interferences (hereinafter "the Board"). A communication dated August 24, 2005, indicates that the file for that application has been forwarded to the Board.

The final rejections in U.S. Application Serial No. 09/997,019, another divisional of the '783 Application, are also the subject of an appeal before the Board. A Notice of Appeal was filed in that application on August 1, 2005.

The undersigned attorney is not aware of any other action, including any other appeals or interferences, currently ongoing before Board that may affect or be affected by the Board's decision in the appeal of the status of the '783 Application.

## III. STATUS OF CLAIMS

The '783 Application was filed with one hundred one (101) claims.

Claims 1-87 remain pending in the '783 Application. Of these, only claims 1-17 have been considered, claims 18-87 having been withdrawn from consideration. Each of claims 1-17 stands rejected.

Claims 88-101 have been canceled without prejudice or disclaimer.

No claims have been allowed.

The rejections of claims 1-17 are being appealed.

## IV. STATUS OF AMENDMENTS

The '783 Application was originally filed with one hundred one (101) claims.

A Preliminary Amendment was mailed on January 31, 2001.

On July 12, 2001, a restriction requirement and an election of species requirement were made. In a response dated July 26, 2001, an election, responsive to the restriction requirement, was made to prosecute claims 1-87 without traverse. In response to the election of species requirement, an election was made to prosecute claims drawn to a method for disposing material on a semiconductor device structure. It was also explained that claim 1, which is generic to the elected specie, is also generic to others of the identified species of invention.

Another restriction and election of species requirement was made on December 10, 2001. A response was mailed on October 16, 2001. In response to the restriction requirement, an election was again made, without traverse, to prosecute claims 1-87. In addition, in response to the election of species requirement, an election was again made to prosecute claims drawn to a method for disposing material on a semiconductor device structure. An explanation was also

provided that claim 1, which is generic to the elected specie, is also generic to several of the other identified species of invention.

On February 28, 2002, in a first Office Action on the merits, only claims 1-17 were considered. Each of these claims was rejected.

An Amendment responsive to the February 28, 2002, Office Action was filed on May 28, 2002. Revisions to several of the considered claims were presented in the Amendment. In addition, claims 88-101 were canceled without prejudice or disclaimer.

A second, Final Office Action was mailed on August 14, 2002. Again, each of claims 1-17 was rejected.

An Amendment Under 37 C.F.R. § 1.116 was mailed on October 7, 2002, and received a filing date of October 15, 2002.

The Office refused to enter the amendments that were presented in the October 15, 2002, amendment, as evidenced by an Advisory Action dated November 19, 2002.

Accordingly, on November 22, 2002, a Request for Continued Examination was filed requesting entry of the amendment previously refused. No further amendments have been presented in the '783 Application.

Thereafter, on December 19, 2002, a third Office Action on the merits was mailed. Despite the amendments that were presented in the October 15, 2002, Amendment Under 37 C.F.R. § 1.116 and the accompanying explanations as to why the pending claims were patentable, each of claims 1-17 was again rejected.

Further remarks were presented in a Response dated March 24, 2003.

The Office responded with a fourth, Final Office Action, which was mailed on June 3, 2003, in which each of claims 1-17 was again rejected.

Yet another attempt was made to convince the Office of the patentability of claims 1-17 in a Response to Final Office Action, mailed on July 29, 2003.

Nonetheless, the Examiner elected to maintain all of the then-pending rejections in an Advisory Action mailed on September 29, 2003.

Upon receiving the Advisory Action, a Notice of Appeal was filed on October 2, 2003. An Appeal Brief, Examiner's Answer, and Reply Brief were also entered into the file for the '783 Application. The application was withdrawn from the appeals process, by way of a Request for Continued Examination (RCE) filed on November 5, 2004, so that the Examiner could consider art that had been cited in a related application.

After the RCE was filed, the Examiner maintained her prior rejections of claims 1-17 in a non-final action dated December 1, 2004, a Final Office Action dated May 12, 2005, and an Advisory Action dated July 26, 2005. Additional explanations as to the patentability of claims 1-17 were provided in responses that were mailed on March 1, 2005, and July 12, 2005.

After several unsuccessful attempts to convince the Examiner of the impropriety of her rejections and of the patentability of claims 1-17, another Notice of Appeal was filed on July 29, 2005.

This Appeal Brief follows the Notice of Appeal and is being filed within two months of the filing date of the Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims that have been considered in the '783 Application are drawn to methods for forming nonplanarized layers on semiconductor device structures. The nonplanarized layers include regions (*e.g.*, portions located over or within at least one recess) with substantially planar surfaces, on semiconductor device structures.

A material is applied to a semiconductor device structure by a known process and is spread across the surface of the semiconductor device structure so as to substantially fill at least one recess of the semiconductor device structure. *See, e.g.*, paragraphs **[0011]**, **[0013]**. The material is applied in such a way that a layer formed therewith is thinner, or nonexistent, over regions of the semiconductor device structure. *See, e.g., id.* By way of example, the thickness of a portion of the layer that overlies or is located within a nonrecessed area of the semiconductor device structure may be about half or less than half of the depth of the recess. *See, e.g., id.* The material may be spread across the surface of the semiconductor device structure by use of spin-on techniques. In spinning the material onto the semiconductor device structure, the material may be applied at a first speed, the rate of spinning decreased to a second speed at which the material is permitted to at least partially set up, then the rate of spinning gradually increased, or ramped up, to a third speed at which a desired, reduced thickness of material covering the surface may be obtained. *See, e.g., id.* The rate at which the semiconductor device capacitor structure is spun may again be decreased to permit the material to further set. *See, e.g., id.* An edge bead of material may then be removed from the semiconductor device structure and the semiconductor device structure spun once again to remove solvents, if any, from the material. *See, e.g., id.*

The methods may be used, by way of example only, to form masks for hemispherical grain (HSG) polysilicon bottom electrodes of capacitor structures, dopant masks for shallow trench isolation structures, stress buffers for subsequent use in planarization processes, and the like. *See, e.g.,* paragraphs **[0010]**, **[0012]**, **[0016]-[0020]**.

## VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether claims 1, 2, 8, 9, 11, 16, and 17 are patentable under 35 U.S.C. § 102(e) for reciting subject matter which is not anticipated by that taught in U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi");

(B) Whether, under 35 U.S.C. § 103(a), claims 3-7 are nonobvious and, thus, patentable over the asserted combination of teachings from Kikuchi and U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara");

(C) Whether claim 10 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over that taught in Kikuchi, in view of teachings from U.S. Patent 6,046,083 to Lin et al. (hereinafter "Lin"); and

(D) Whether each of claims 12-15 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over that taught in Kikuchi, in view of the teachings of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park").

## VII. ARGUMENT

### A. REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1, 2, 8, 9, 11, 16, and 17 stand rejected under 35 U.S.C. § 102(e).

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

M.P.E.P. § 2112 explains the inherent description provided by a reference as follows:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency of that result or characteristic. *In re Rijckaert,* 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) . . . 'To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill . . .'' *In re Robertson,* 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1991).

2. REFERENCE RELIED UPON

A summary of the pertinent teachings of Kikuchi, which has been relied upon in the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17, follows:

*Kikuchi*

Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 has been disposed within and over a via-hole 23a. Kikuchi also discloses that

the resist 20 can be applied by several conventional methods, including spin-coating. Col. 17, lines 63-66.

While resist 20 *appears* in Fig. 6D of Kikuchi to have a planar surface, Kikuchi lacks any express or inherent description that the surface of resist 20 is planar.

3. ANALYSIS

Independent claim 1 recites a method for disposing a material on a semiconductor device structure. In the method of independent claim 1, material is disposed on a surface of a semiconductor device structure "so as to substantially fill . . . at least one recess [thereof, the] material covering [the] surface having a thickness less than a depth of said at least one recess . . ." A material layer with these characteristics is formed "without subsequently removing [the] material from [the] surface . . ." Independent claim 1 also requires that "an upper surface of at least a portion of said material over or within said at least one recess [be] substantially planar."

There is no need for a quantifiable dimensional range for the phrase "substantially planar" in independent claim 1 since one of ordinary skill in the art would readily understand the meaning of the phrase "substantially planar" in reference to the planarity of the upper surface of a particular type of material that has been disposed within or over a recess of a semiconductor device structure. *See, e.g.,* M.P.E.P. § 2173.05(b).

It is respectfully submitted that Kikuchi does not anticipate a method that includes disposing material in such a way that "an upper surface of at least a portion of [the] material over or within . . . at least one recess [is] substantially planar."

While it has been asserted that Fig. 6D of Kikuchi shows a layer of resist 20 which *appears* to have a planar surface, it is respectfully submitted that Kikuchi, in fact, lacks any express description that the surface of resist 20 is planar. A high standard has been set for reliance on drawings in prior art rejections. In view of the warning that has been provided by M.P.E.P. § 2125 with respect to reliance upon the drawings of a patent, and without further guidance from the specification of Kikuchi, the mere inclusion of a straight line to depict the surface of resist 20 does not adequately indicate that surfaces represented by the straight lines are substantially planar. Thus, Kikuchi does not expressly or inherently describe that any portion of the surface of resist 20 or, more specifically, that the surface of the portion of resist 20 that is over or within recesses, is substantially planar.

Moreover, Kikuchi includes no express or inherent description that the thickness of portions of the resist that cover the surface of the illustrated semiconductor device structure are less than a depth of at least one resist-filled recess therein. As has been established, the drawings of Kikuchi are merely simplified representations that cannot be relied upon to support the assertion that Kikuchi discloses a particular thickness of resist over a semiconductor device structure relative to the depth of a recess in the semiconductor device structure.

It is also respectfully submitted that Kikuchi lacks any inherent description that the method described therein results in a layer of resist 20 that includes a portion over or within a recess with a planar surface. As would be readily apparent to those of ordinary skill in the art, it is clear that the conventional spin-on processes and photoresist material employed in Kikuchi do not necessarily result in a planar surface on resist 20 which is disposed over or within via-holes 23a. As pointed out by the "Background" section of the specification of

the '783 Application, at page 3, line 15, to page 4, line 29, the limitations in previously known spin-on methods, as well as material properties (*e.g.,* viscosity, solids content, surface tension, adherence to adjacent materials, etc.), may prevent a layer of material, such as the resist 20 disclosed by Kikuchi and illustrated in Fig. 6D, from having a substantially planar upper surface. *See, e.g.,* Van Zandt, P., Microchip Fabrication – Chapter 8, Photolithography—Preparation to Exposure, pages 176-178 and 185-187 (hereinafter "Van Zandt"). Further, Van Zandt, at page 185, evidently recognizing that a spun-on layer of photoresist will include valleys that are located over recesses in a semiconductor substrate, describes spun-on photoresist in terms of *layer* thickness (*e.g.,* 0.5 μm to 1.5 μm thick, with variations of ± 0.01 μm) rather than in terms of surface planarity. U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara") provides further evidence that the surfaces of spun-on photoresist layers may not be planar. Yoshihara, col. 1, line 18, to col. 2, line 17).

Based on the aforementioned background art, coupled with the law relating to anticipation and Kikuchi's aforementioned deficiencies, no speculation or misconstruction of the disclosure of Kikuchi is necessary to state that Kikuchi lacks any express or inherent description of a method that includes disposing resist 20 on a surface of a semiconductor device structure 21 such that the resist 20 over or within a via-hole 23a thereof has an upper surface which is substantially planar. Rather, it is the Office's assertions that Kikuchi does anticipate such subject matter that are based on mere speculation as to the nature of the surface of resist 20 over wor within via-holes 23.

For these reasons, it is respectfully submitted that Kikuchi does not anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e). Thus, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Kikuchi.

Claims 2, 8, 9, 11, 16, and 17 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2 should be construed in accordance with its plain language, as well as the equivalents thereto, and should not be limited to the examples of structures shown in Figs. 2 and 3 of the '783 Application.

Claim 2, which is rejected as being anticipated by Figs 6A-6E; 10A-10E; 13A-13E, is further allowable since none of these figures shows "disposing [a] material . . . so as to substantially fill . . . at least one recess *without substantially covering* [a] surface of a semiconductor device structure . . ." While the various figures that have been referenced in support of this assertion, including Figs. 6E, 10D, 10E, and 13E of Kikuchi, show structures which include recesses that are substantially filled with material while the same material does not cover the surfaces of the illustrated semiconductor devices, these structures are not formed while *disposing* material. Rather, Kikuchi describes that conventional resist application techniques are used, then, after *disposing* the resist, *removing* excess resist by *another, subsequent process*. For example, etchants may be used in the conventional processes described in Kikuchi to remove excess material (col. 18, lines 3-5; col. 26, lines 19-21; col. 40, line 66, to col. 41, line 1), or a positive photoresist may be applied, then exposed to electromagnetic radiation, from which portions of the photoresist within recesses are shielded (col. 18, lines 5-8; col. 35, lines 40-52), with exposed and developed portions of the photoresist being subsequently washed away. Thus,

Kikuchi neither expressly nor inherently describes "disposing" a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses "without substantially covering [the] surface."

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 3-7, 10, and 12-15 stand rejected under 35 U.S.C. § 103(a).

1. APPLICABLE LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. ADDITIONAL REFERENCE RELIED UPON

A summary of the pertinent teachings of Yoshihara, which has been relied upon in the 35 U.S.C. § 103(a) rejections of claims 3-7, follows:

*Yoshihara*

Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm"; col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that the material layer has a substantially uniform thickness. The phrase "uniform thickness" should not be confused with a "substantially planar" upper surface.

3. ANALYSIS

(a) KIKUCHI IN VIEW OF YOSHIHARA

Claims 3-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of Yoshihara.

It is respectfully submitted that claims 3-7 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is itself allowable.

Moreover, neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art would have motivated one of ordinary skill in the art to combine teachings from Kikuchi with teachings from Yoshihara to arrive at the inventions to which claims 3-7 are drawn. Kikuchi teaches that layers of resist may be spin-coated onto semiconductor substrates that include recesses. As is well known in the art, conventional spin-coating processes result in resist

layers which have substantially uniform thicknesses; a teaching which is not contradicted by Kikuchi. However, Kikuchi neither teaches nor suggests that resist layers so formed have substantially planar surfaces, at least over or within the recesses of such semiconductor substrates. Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm"; col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that the material layer has a substantially *uniform thickness*. It is clearly not possible for a layer which has a substantially uniform thickness and which is formed over a nonplanar surface to have a planar surface. It is, therefore, respectfully submitted that Yoshihara does not supply the motivation, suggestion, or teaching missing from Kikuchi that the techniques described in Kikuchi or Yoshihara are useful for disposing material within recesses such that the upper surface of at least the material within or over the recesses has a substantially planar upper surface.

As neither of these references teaches or suggests that resist or any other material within recesses of a semiconductor device structure may have a planar surface, as required by independent claim 1, it is respectfully submitted that the only way one of ordinary skill in the art could have been motivated to combine the teachings of these references in such a way as to render obvious a method which includes disposing material within a recess so that the material has a substantially planar surface would have been to improperly glean such motivation from the description of the '783 Application.

Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Kikuchi and Yoshihara in the manner that has been asserted.

It is also respectfully submitted that the asserted combination of teachings from Kikuchi and Yoshihara does not teach or suggest each and every element of claim 5. In particular, neither Kikuchi nor Yoshihara teaches or suggests initially spinning a semiconductor device structure at a rate of about 1,000 rpm, as recited in claim 5. Instead, the initial spin rate taught by Yoshihara is "as low as 2000 rpm . . .," which is more than twice as high as the initial rate recited in claim 5. Col. 11, line 16.

In view of the foregoing, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 3-7. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 3-7 is allowable over the combination of Kikuchi with Yoshihara.

(b) KIKUCHI IN VIEW OF LIN

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,046,083 to Lin et al. (hereinafter "Lin").

It is respectfully submitted that claim 10 is allowable, among other reasons, as depending from claim 1, which is allowable.

(c) KIKUCHI IN VIEW OF PARK

Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park").

It is respectfully submitted that claims 12-15 are allowable, among other reasons, as depending either directly or indirectly from claim1, which is allowable.

For these reasons, reversal of the 35 U.S.C. § 103(a) rejections of claims 3-7, 10, and 12-15 is respectfully requested.

## VIII. ELECTION OF SPECIES REQUIREMENTS

It is respectfully submitted that, as independent claim 1 remains generic to all of the species of invention that have been identified by the Office, claims 18-87 should be brought back into consideration in the '783 Application and allowed for the reasons that have been provided herein. M.P.E.P. § 806.04(d).

## IX. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '783 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

## X. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

## XI. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XII. CONCLUSION

(A) Claims 1, 2, 8, 9, 11, 16, and 17 are allowable under 35 U.S.C. § 102(e) for reciting subject matter which is not anticipated by that the subject matter taught in Kikuchi;

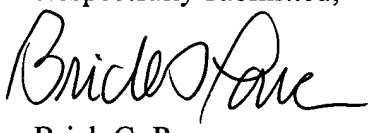
(B) Claims 3-7 are nonobvious under 35 U.S.C. § 103(a) and, thus, allowable over the asserted combination of teachings from Kikuchi and Yoshihara;

(C) Claim 10 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over that taught in Kikuchi, in view of teachings from Lin; and

(D) Each of claims 12-15 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is allowable over that taught in Kikuchi, in view of the teachings of Park.

Accordingly, reversal of the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 and of the 35 U.S.C. § 103(a) rejections of claims 3-7, 10, and 12-15 is respectfully requested, as is the allowance of claims 1-87.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: September 29, 2005

BGP/djp:eg
Document in ProLaw

## CLAIMS APPENDIX

1. A method for disposing a material on a semiconductor device structure, comprising:

providing a semiconductor device structure including a surface and at least one recess formed in said surface;

disposing said material on said surface so as to substantially fill said at least one recess, said material covering said surface having a thickness less than a depth of said at least one recess without subsequently removing said material from said surface, an upper surface of at least a portion of said material over or within said at least one recess being substantially planar.

2. The method of claim 1, wherein said disposing comprises disposing said material so as to substantially fill said at least one recess without substantially covering said surface.

3. The method of claim 1, wherein said disposing comprises:

applying said material to said surface of said semiconductor device structure;

spinning said semiconductor device structure;

decreasing a rate of said spinning while permitting said material to at least partially cure; and

gradually increasing said rate of said spinning.

4. The method of claim 3, further comprising exposing said material to a soft baking temperature following said gradually increasing.

5. The method of claim 3, wherein said spinning is effected at a rate of about 1,000 rpm.

6. The method of claim 3, wherein said decreasing said rate comprises decreasing said rate of said spinning to about 100 rpm.

7. The method of claim 3, wherein said gradually increasing said rate comprises gradually increasing said rate of said spinning to at least about 1,000 rpm.

8. The method of claim 1, wherein, upon exposing said material disposed over an entirety of said semiconductor device structure to an etchant, said material covering said surface is substantially removed therefrom, while said material located in said at least one recess substantially fills said at least one recess.

9. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material.

10. The method of claim 9, wherein said providing said semiconductor device structure comprises providing said stacked capacitor structure with said surface and said at least one container being lined with doped hemispherical grain polysilicon.

11. The method of claim 9, wherein said disposing said material comprises disposing a mask material over said semiconductor device structure.

12. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

13. The method of claim 12, wherein said disposing said material comprises disposing a mask material over said shallow trench isolation structure.

14. The method of claim 12, wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface.

15. The method of claim 14, wherein said disposing said material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

16. The method of claim 1, wherein said providing comprises providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material with a nonplanar surface disposed in said at least one dual damascene trench and at least partially covering said surface.

17. The method of claim 16, wherein said disposing said material comprises disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

18-87. (Withdrawn)